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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PETRANEK, JACOB ANDREW	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	08/966,954	GERARDUS DE VRIES, JOHANNES R.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *44,45,49 and 63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *44,45,49 and 63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 44, 45, 49, and 63 are pending.

2. The office acknowledges the following papers:

Specification, claims, arguments, and drawings filed on 10/31/2007.

Withdrawn objections and rejections

3. The drawing objections have been withdrawn due to amendment.

New Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 44, 45, 49, and 63 are rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The limitation from claims 44 and 63 "Each of the at least three functional units having an input coupled directly to one of the at least three dedicated output buses" is not enabled within the specification upon a cursory glance. The specification doesn't detail how the output bus of a functional unit can be directly connected to an input of a functional unit. Allowing such a limitation results in a plurality of outputs from functional units fed directly back into the functional units regardless of if they are needed for

execution or not. The claimed limitation allows for no way of being able to not feed back execution results to the functional units when they are not needed. Thus, the specification fails to enable one of ordinary skill in the art how the invention would work when such bypassing is not needed by the functional unit to execute an instruction without undue burden or experimentation.

6. Claims 44, 45, 49, and 63 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The limitation from claims 44 and 63 "A second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units" is not contained within the specification upon a cursory glance. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The limitation from claims 44 and 63 "Each of the at least three functional units having an input coupled directly to one of the at least three dedicated output buses" is not contained within the specification upon a cursory glance. Specifically, looking at figure 3 of the drawings, separate dedicated output buses from the ALU, multiplier, and shift register are directly coupled to a register. Thus, the separate dedicated output

buses can't be directly connected to an input of the ALU, multiplier, and shift register in figure 3. Thus, the claimed limitation was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

7. Claims 45 and 49 are rejected due to their dependency.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 44, 45, 49, and 63 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation from claims 44 and 63 "Each of the at least three functional units having an input coupled directly to one of the at least three dedicated output buses" is not enabled within the specification upon a cursory glance. The specification doesn't detail how the output bus of a functional unit can be directly connected to an input of a functional unit. Allowing such a limitation results in a plurality of outputs from functional units fed directly back into the functional units regardless of if they are needed for execution or not. The claimed limitation allows for no way of being able to not feed back execution results to the functional units when they are not needed. For examination purposes, the claimed limitation will be interpreted as "Each of the at least three functional units having an input coupled [[directly]] indirectly to one of the at least three dedicated output buses," which is shown in figure 3 having a plurality of different

components between the output bus of a functional unit and an input to the functional unit.

10. Claims 45 and 49 are rejected due to their dependency.

New Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 44, 45, 49, and 63 are rejected under 35 U.S.C. §103(a) as being unpatentable over Chuang (U.S. 4,766,566), in view of Labrousse et al. (U.S. 5,313,551), in view of Yokouchi (U.S. 4,958,275), in view of Blahut et al. (U.S. 4,346,437).

13. As per claim 44:

Chuang disclosed a processor comprising:

At least three functional units coupled to each other to execute operations defined from an instruction set of the processor (Chuang: Figure 7 elements 24, 60, 62, and 70, column 10 lines 18-41), the at least three functional units including an arithmetic logic unit (ALU) and a multiplier (Chuang: Figure 7 elements 24, 60, 62, and 70, column 10 lines 18-41), the instruction set having a hierarchy of instruction levels, each of which can be used by a programmer to define instructions for the processor, the hierarchy of instruction levels including:

A RISC/CISC assembly code level (Chuang: Figure 7, column 5 lines 3-20)(The processor of figure 7 executes RISC instructions.), and

A bus routing structure that includes at least three dedicated output buses, including a separate dedicated output bus for each of the at least three functional units, each of the at least three dedicated output buses being dedicated to convey data output by a separate one of the at least three functional units, each of the at least three functional units having an input coupled indirectly to one of the at least three dedicated output buses (Chuang: Figure 7 elements 24, 60, and 70)(Elements 24, 60, and 70 are three functional units with three separate dedicated output buses to convey output data. These output buses are indirectly coupled to the inputs of elements 24, 60, and 70 via the output registers, register file, and input registers.).

Chuang failed to teach a second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units.

However, Labrousse disclosed a second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units (Labrousse: Column 13 lines 35-42 and column 14 lines 17-22)(The instructions that contain bypass encoding signals are available to the programmer and are implemented into the instructions upon being compiled. Labrousse disclosed instructions that can be encoded with a bypass signal that can be used to bypass register reads without having a make a comparison between addresses for instructions.).

The advantage of encoding bypass signals within an instruction is that it will save the time needed to make comparisons between source registers between instructions and it will save space on the processor, which will lower costs (Labrousse: Column 2 lines 56-62). Allowing for bypass in the instruction will also result in the register value being available sooner to the instruction needing it, which may increase performance if the register access is in the critical path (Labrousse: Column 1 lines 49-64). The advantages of saving processor space and power, as well as increased performance would have motivated one of ordinary skill in the art to implement directly encoding bypass signals into instructions to execute. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement encoding bypass signals into instructions for the advantages of increased performance and decreased costs.

Chuang and Labrousse failed to teach a vector processing assembly code level, using which an individual instruction can be automatically repeated a programmable number of times on different data words; and a plurality of control registers, the plurality of hierarchical instruction levels further comprising a fourth level corresponding to the control registers, using which individual instruction words executed by one or more of the functional units can be extended by bits in the control registers on a per-instruction-cycle basis.

However, Yokouchi disclosed a vector processing assembly code level, using which an individual instruction can be used to cause an operation to be automatically repeated sequentially a programmable number of times on different data words (Yokouchi: Figure 1 element 23, column 6 lines 7-19 and column 9 lines 15-67

continued to column 10 lines 1-3)(A vector operation is defined as an operation where a large number of data words are subjected to the same arithmetic operation. Element 23 is the execution unit that repeatedly executes the ADDC instruction in table 2. The number of times the ADDC instruction is repeated is set by the MOVMOD instruction in table 2. The ADDC instruction repeats the programmed number of times on different data. The claim currently doesn't require that the repeat instruction includes a count number indicating the number of repeats. However, if it did, combining the MOVMOD and ADDC instruction would be obvious to one of ordinary skill in the art for the advantage of increased performance by eliminating an instruction and reducing the program size. In addition, according to "In re Larson" (144 USPQ 347 (CCPA 1965)), to make integral doesn't give patentability over prior art.).

The advantage of a repeat instruction is that it allows for high processing speed and a high byte efficiency (Yokouchi: Column 9 lines 63-67 continued to column 10 lines 1-3). The repeat instruction over the conventional code structure shown in table 2 also is more compact, which allows for the code segment to be executed quicker and results in increased performance. One of ordinary skill in the art at the time of the invention would have been motivated by these advantages to implement a repeatable instruction onto the processor of Chuang and Labrousse. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a repeatable instruction for the advantages of increased performance.

Chuang, Labrousse, and Yokouchi failed to teach a plurality of control registers, the plurality of hierarchical instruction levels further comprising a fourth level

corresponding to the control registers, using which individual instruction words executed by one or more of the functional units can be extended by bits in the control registers on a per-instruction-cycle basis.

However, Blahut disclosed a plurality of control registers, the plurality of hierarchical instruction levels further comprising a fourth level corresponding to the control registers, using which individual instruction words executed by one or more of the functional units can be extended by bits in the control registers on a per-instruction-cycle basis (Blahut: Elements 31 and 33, column 8 lines 42-62)(Elements 31 and 33 make up the plurality of control registers, with element 33 being directed towards instruction extension. The programmer is allowed to load data into a control register that allows for the extension of instructions within the processor. The extension can be on a per instruction basis because the programmer controls when the control register is loaded and reloaded to allow for instruction extension. When element 33 is loaded, each instruction is affected on an per-instruction-cycle basis.).

The advantage of using a control register for instruction extension is that it allows for additional instructions to be executed within the processor. Many times, instruction opcodes may all be used, thus using a control register is a way that additional instructions can be added to the processor (Blahut: Column 1 lines 61-67 continued to column 2 lines 1-67). One of ordinary skill in the art would have been motivated to implement control registers for the advantage of allowing the instruction set architecture to increase, even though no more opcode values may exist. Thus, it would have been obvious to one of ordinary skill in the art to implement control registers for extending

instructions for the advantage of being able to add additional functionality to the processor.

14. As per claim 45:

Chuang, Labrousse, Davies, and Blahut disclosed a processor as recited in claim 44, wherein the second assembly code level comprises a native machine language of the processor (Labrousse: Column 13 lines 35-42 and column 14 lines 17-22)(The instructions that contain bypass encoding signals are available to the programmer and are implemented into the instructions upon being compiled. Labrousse disclosed instructions that can be encoded with a bypass signal that can be used to bypass register reads without having a make a comparison between addresses for instructions. The instructions are inherently native to the processor upon the combination and can be used by the processor.).

15. As per claim 49:

Chuang, Labrousse, Davies, and Blahut disclosed a processor as recited in claim 44, further comprising:

At least three bus registers, each coupled to store the output of only a corresponding one of the at least three functional units and each coupled to only a corresponding one of the at least three dedicated output buses (Chuang: Figure 7 elements 66 and 68, column 10 lines 18-41)(The two output registers are coupled to the functional units and the output buses. It's obvious to one of ordinary skill in the art that an additional execution unit can be added to Chuang to allow for increased parallel execution, which would result in a third bus register. The advantage of adding a third

execution unit would allow for increased performance through additional parallel execution in the processor of Chuang. Additionally, this would be obvious to one of ordinary skill in the art at the time of the invention since Chuang's main purpose of the invention is to add additional parallel execution, by adding a second execution unit to execute instructions in parallel (see figures 4 and 7). In addition, according to "In re Rose" (105 USPQ 237 (CCPA 1955)), changing in size/range doesn't give patentability over prior art.).

16. As per claim 63:

Claim 63 essentially recites the same limitations of claims 44-45 and 49. Therefore, claim 63 is rejected for the same reasons as claims 44-45 and 49.

Response to Arguments

17. The arguments presented by Applicant in the response, received on 10/31/2007 are not considered persuasive.

18. Applicant argues "Written description support for the limitation "a second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units" is found particularly in paragraph 46, especially in table 1 and the notes at the end of table 1."

This argument is not found to be persuasive for the following reason. The examiner still isn't fully convinced that this limitation has support even within table 1 and

the end notes. Table 1 only shows instructions referencing primarily two registers, R and S. Thus, table 1 by itself clearly doesn't show support for the claimed limitation.

Additionally, the applicant alleges support from the notes at the end of table one. The end notes at the end of table 1 only state that the two operands **can** be selected from a plurality of busses (emphasis added). However, this is an inherent feature in any processor that performs bypassing. A processor with bypassing can select an operand from a bypass bus or select an operand from a register file. Thus, the processor is capable of selecting from a plurality of bus sources, as shown at the end of table 1.

However, there isn't any mention in paragraph 46 that a programmer can explicitly reference individual outputs, which would allow a programmer to put, for example, an instruction in a program such as "Add A, B (bypass selected from data-memory bus), C (bypass selected from ALU)." To have support for this limitation, the specification must say that the programmer can explicitly reference bypass busses in an instruction.

Finally, the applicant appears to state that there's no explicit support in the specification with the statement:

> As previously mentioned, the note immediately following table 1 expressly states that operands R and S each can be selected from the various different buses, A (register), D (data-memory), M (multiplier) and Q (barrel-shifter). Furthermore, when read in conjunction with the rest of the description, particularly Figure 3 and its associated text, there would be absolutely no doubt in the mind of a person of ordinary skill in the art that what is being described includes an assembly code level (the "free pipeline" level) which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units.

The examiner strongly disagrees that one of ordinary skill in the art would find it obvious that the specification in paragraph 46 and figure 3 supports allowing a programmer to directly bypass operands within instructions without explicit support within the specification. This is especially the case since one of ordinary skill in the art would known that bypassing is usually done in hardware and not software. Thus, there's no reason for one of ordinary skill in the art to take away that the bypassing is done in software by the programmer and not by hardware without explicit support stating that this is the case.

19. Applicant argues "Chuang failed to teach a bus routing structure that includes at least three dedicated output buses, including a separate dedicated output bus for each of the at least three functional units, each of the at least three dedicated output buses being dedicated to convey data output by a separate one of the at least three functional units, each of the at least three functional units having an input coupled directly to one of the at least three dedicated output buses."

This argument is not found to be persuasive for the following reason. The examiner rejected the claim under both 112 1st and 2nd paragraph and interpreted the claim in view of figure 3 stating figure 3. The examiner interpreted the limitation as at least three functional units having an input coupled indirectly to one of the at least three dedicated output buses. Chuang disclosed three function units, elements 24, 60, and 70, which output data on the output of each element. This output is considered the dedicated output bus for each of the functional units. These buses are able to indirectly fed the inputs of the functional units through the output register, register file, input

registers, and FMT (only for the ALU's), as shown in figure 7. Thus, Chuang reads upon the interpreted claimed limitation.

Applicant is correct in the assumption that "the output of the various units in Chuang's Fig. 7 (e.g., multiplier 63, output register 68, etc.) can be considered dedicated output buses of the functional units," except that the output of the output registers (Figure 7 elements 66 and 68) aren't being read as the dedicated output buses. Only the outputs of the functional units are.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner, Art Unit 2183

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